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In Chapters 4 and 5 we considered the techniques for regular realization of complex control automata on a chip (matrix realization) and for synthesis of their logic circuits with programmable logic arrays with and without memory. In this chapter we concentrate on the multilevel minimization of the control automaton logic circuits with gates.

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In temporal logic, it may be simply written as a conjunction of the following two formulae: 1) $[r1 \wedge i2 \rightarrow \neg u2Ui1]$, 2) $[r2 \wedge i1 \rightarrow \neg u1Ui2]$. The first formula may be paraphrased as 'whenever USER1 requests to use the resource when USER2 is idling (i.e., $r1 \wedge i2$ is true), USER2 will not be allowed to use it (i.e., $u2$).

Integrating Temporal Logic as a State-Based Specification ...

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